COMP 260: Digital Logic and Computer Design (Section 001)
Fall 2004 Course Information & Syllabus

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Lectures: TR 11:30am–12:45pm in 25EP-0206.
Sometimes lecture notes or a summary will be available on the web. Other than that, if you have to miss a class, get notes from another student; mine are typically pieced together from more than one place with a lot of metacomments, which makes it hard for anybody but me to follow them. Also get copies of any missed handouts (available on the web site). The handouts are numbered sequentially, starting with handout 0. On handout 0, you need to fill in some information and return it to me promptly so you can be on the email list and get access to the web site for the course.

Office Hours: In Lewis Towers 512E: 10:30–11:30 and 2:15–3:00 on Tuesday and Thursday.
These are the guaranteed times to find me except as announced in advance. You should also be able to find me at lots of other times; feel free to look for me or make appointments.

Course Objectives: This course is designed to provide a basic understanding of how a computer works. The course will begin at the level of digital logic and circuit design and proceed to the high-level organization of a computer.

Prerequisites: COMP 170.

Required Text: Required Text: John D. Carpinelli. *Computer System Organization and Architecture*. Addison Wesley, 2001.

Course Requirements: There will be homework and/or in-class exercises, four tests, and a final. The weightings within the semester grade will be: Homework & class participation: 15%, Test 1: 12%, Tests 2–4: 16% each, and Final exam 25%.

Homework: Only homework turned in by the due date is guaranteed to be graded. Any special circumstances that cause difficulty in meeting the deadlines should be brought to the attention of the instructor in advance. Homework must be handed in at the beginning of class, since solutions may be handed out in the same class on occasion. Homework turned in to my mailbox will generally not be graded, since I do not check the box continually and cannot generally verify that homework was turned in before solutions were distributed or discussed in class. If you cannot turn in homework in person, you should put it under the door of my office.

Exams: The schedule tentatively calls for four 50 minute tests in week 5, week 9, week 11, and week 15. The final exam is scheduled for 8:30–10:30 am on Thursday, December 16.

Collaboration: *No* collaboration is permitted on exams. *Collaboration* on homework is acceptable, but *copying* is not! (Safeguard your files and printouts.) You may discuss solution techniques with other students, but you must write up your solutions independently. If you obtain a solution through research, e.g., in the library, credit your source and write up the solution in your own words.

Tentative Course Outline and Approximate Schedule:

Recommended readings from the text are shown on a weekly basis. (When selected sections or subsections are listed, it is assumed that you will include the introduction of the corresponding chapter or section.)

1. (8/31) Digital logic and Boolean algebra. Section 1.1.
2. (9/7) Karnaugh maps. Section 1.1.
   Combinational Circuits. Sections 1.2-1.3.
3. (9/14) Sequential circuits. Sections 1.5–6.
4. (9/21) Finite-state machines. Sections 2.1–3.
   Instruction set architectures. Sections 3.1–3.
5. (9/28) Catch up on lecture material, problem solving and review for Exam 1.
   Exam I on Chapters 1–2.
6. (10/5) A simple instruction set. Section 3.4.
7. (10/14) Basic computer organization. Section 4.1.
   CPU, memory, and I/O organization and interfacing. Sections 4.2–5. Will spill over to 10/19.
8. (10/19) Catch-up on past lecture material.
   Register transfer languages. Sections 5.1–3.
9. (10/26) Exam II on Chapters 3–4.
   CPU design. Sections 6.1–2.
10. (11/2) CPU Design continued. Sections 6.2–4.
11. (11/9) Microprogrammed control unit design. Sections 7.1–2.
    Exam III on Chapters 5–6.
12. (11/16) Fixed point number representations and arithmetic. Sections 8.1.1, 8.2.1.1, 8.2.2, and 8.3.1–2.
13. (11/23) Floating point number representation and arithmetic. Sections 8.5.1–3 and 8.6.
14. (11/30) Memory hierarchy. Sections 9.1–2.
    Virtual memory. Sections 9.3.1–3
15. (12/7) Exam IV on Sections 7.1–9.2.
    Review for final exam.