Malloc & VM

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Agenda

Administration

- Process lab code will be inked by Thursday (pick up in ECE hub)
- Malloc due soon (Thursday, November 4th)
- Exam 2 in a week (Tuesday, November 9th)
- Proxy Lab out in a week (Tuesday, November 9th)

Plan for today

- Finish malloc questions
- mm checkheap
- VM

Malloc

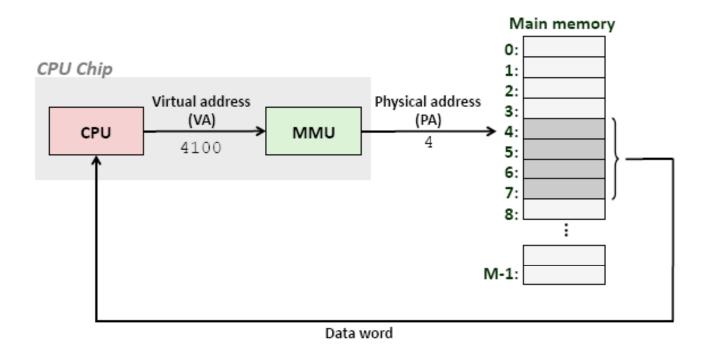
Questions?

mm_checkheap

- More for YOU than for US.
 - But we'll grade it.
- Checks consistency of data structure
 - (Doubly) linked lists are pointed correctly?
 - Headers and footers match up?
 - No allocated blocks in your explicit list?
 - No free blocks NOT in your explicit list?
 - Any of YOUR OWN invariants! (address-ordering?)
 - Seg lists: no big chunks in small lists / vice versa?

Virtual Memory

A System Using Virtual Addressing



- Used in all modern servers, desktops, and laptops
- One of the great ideas in computer science

Carnegie Mellon

Review of Symbols

Basic Parameters

- N = 2ⁿ: Number of addresses in virtual address space
- M = 2^m: Number of addresses in physical address space

Basic Concepts

P = 2^p : Page size (bytes)

Components of the virtual address (VA)

- TLBI: TLB index
- TLBT: TLB tag
- VPO: Virtual page offset
- VPN: Virtual page number

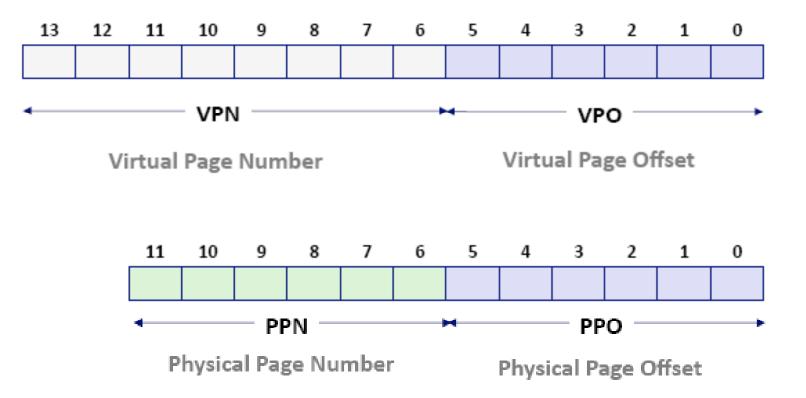
Components of the physical address (PA)

- PPO: Physical page offset (same as VPO)
- PPN: Physical page number
- CO: Byte offset within cache line
- CI: Cache index
- CT: Cache tag

- Assumptions
 - n-bit virtual address
 - m-bit physical address
 - $-P = 2^p = Page size$
- How big is...
 - The virtual page number?
 - The physical page number?
 - The virtual page offset?
 - The physical page offset?

- Assumptions
 - n-bit virtual address
 - m-bit physical address
 - $-P = 2^p = Page size$
- How big is...
 - The virtual page number? (n-p) bits
 - The physical page number? (m-p) bits
 - The virtual page offset?
 p bits
 - The physical page offset? p bits

- Anatomy of addresses (using 14-bit VA, 12-bit PA, 64 byte page size)
 - The VPN needs to have enough information so that the TLB can look up a PPN for it.
 - The PPN needs to have enough information so that the cache can look up the DATA at the given address.



- These addresses are stored as Page Table
 Entries in a Page Table.
 - Just a listing of conversions from VPN -> PPN
 - And whether it's valid

 Since memory translations happen very often, modern architectures speed this up with a TLB.

- Translation Lookaside Buffer
 - Hardware!
 - Is like a cache from VPNs to PPNs
 - During a translation, ask the TLB first by giving it an INDEX and TAG
- How big is...
 - The index?
 - The tag?

TLB

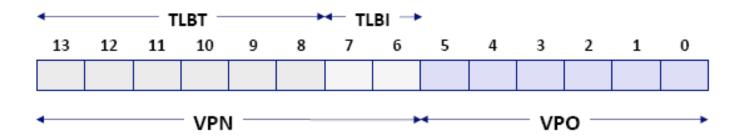
- Translation Lookaside Buffer
 - Hardware!
 - Is like a cache from VPNs to PPNs
 - During a translation, ask the TLB first by giving it an INDEX and TAG
- How big is...
 - The index? log₂ (# of sets)
 - The tag? (n p index_size)

TLB

- TLB Hit
 - Got away with the shortcut!
- TLB Miss
 - Not necessarily a page fault!
 - Go check the page table, and then come back and fill in the missing spot in TLB.
- TLB Miss and not in the page table
 - Page fault. What does the OS do?
 - Make some mappings?
 - Throw a SIGSEGV?
 - Kill the process?

Virtual Address Anatomy

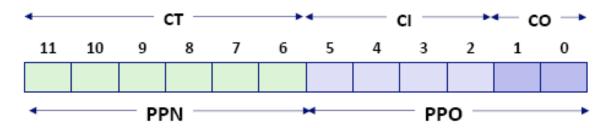
TLB has 4 sets, 14-bit VA, 64 byte pages



Set	Tag	PPN	Valid									
0	03	-	0	09	0D	1	00	_	0	07	02	1
1	03	2D	1	02	-	0	04	_	0	0A	-	0
2	02	-	0	08	-	0	06	-	0	03	-	0
3	07	-	0	03	0D	1	0A	34	1	02	-	0

Physical Address Anatomy

 Direct-mapped cache has 16 lines, each block has 4-bytes. 12-bit PA, 64 byte pages



ldx	Tag	Valid	В0	B1	B2	В3
0	19	1	99	11	23	11
1	15	0	-	-	_	-
2	1B	1	00	02	04	08
3	36	0	-	-	_	_
4	32	1	43	6D	8F	09
5	0D	1	36	72	F0	1 D
6	31	0	_	_	_	_
7	16	1	11	C2	DF	03

ldx	Tag	Valid	В0	B1	B2	В3
8	24	1	3A	00	51	89
9	2D	0	-	-	-	-
Α	2D	1	93	15	DA	3B
В	0B	0	-	-	_	-
С	12	0	-	-	_	-
D	16	1	04	96	34	15
E	13	1	83	77	1B	D3
F	14	0	-	-	_	_

Translation!

End-to-end translation in the book from pages
 794 to 798

Practice!

- Lots of VM questions in past Exam 2s
 - Means you're likely to see one on this test!